Claims 1 and 4 stand objected to in paragraph 5 of the Office Action. It is respectfully submitted that this objection has been addressed and overcome herein.

Claim 1

Claim 1 stands rejected under 35 U.S.C. Section 102(e) as being allegedly anticipated by Hieda (US 6,335,241). This Section 102(e) rejection is respectfully traversed for at least the following reasons.

Claim 1 requires "forming an insulation film and then an adhesion film on the plug and the barrier film, and then forming a hole in the insulation film and the adhesion film leading to the plug such that an upper surface of the plug and an adjacent part of the barrier film are exposed; forming a first conductive film on the insulation and adhesion films and on and over an exposed part of the barrier film in the hole such that the hole in the insulation film and in the adhesion film is filled with the first conductive film, and then etching the first conductive film and the adhesion film by a chemical mechanical polishing method to thereby form a lower electrode within the hole in the insulation film . . . . wherein the adhesion film is removed before the lower electrode is left in the protuberant manner."

For example, see Fig. 1 of the instant application which illustrates adhesion film 11. In the example Fig. 1 embodiment of the instant application, insulation film 6 and then adhesion film 11 are formed on the plug (4 and/or 5) and the barrier film 3. Then, hole 6a is formed in both the insulation film 6 and the adhesion film 11 leading to the plug 4/5 such that an upper surface of the plug and an adjacent part of the barrier film are exposed. Thereafter, a first conductive film 7 is formed on the insulation and adhesion

films 6 and 11, respectively, and on and over an exposed part of the barrier film 3 in the hole 6a such that the hole 6a in the insulation film and in the adhesion film is filled with the first conductive film 7. Then, the conductive film 7 and adhesion film 11 are subject to CMP to form a lower electrode 8 within the hole in the insulation film. The adhesion film 11 is removed before the lower electrode is left in the protuberant manner as shown in Fig. 1D.

The adhesion film required by claim 1 is formed on the first insulation film in order to provide good adhesion between the insulation film and the first conductive film (e.g., to provide good adhesion between insulation film 6 and first conductive film 7 as shown in Fig. 1B of the instant application) (e.g., pg. 11, lines 6-12; pg. 15, lines 9-13; and pg. 20, lines 10-15). Generally speaking, the lower electrode material has poor adhesion to the insulation film. Therefore, without the claimed adhesion film set forth in claim 1, the first conductive film may become detached from the insulation film during the claimed CMP process thereby leading to product failure. Thus, it can be seen that providing the claimed adhesion film between the insulation film and the electrode solves a significant problem in the art, and leads to a much improved product with better yields.

The cited art fail to disclose or suggest the aforesaid underlined aspects of claim 1; in particular the adhesion film and the steps taken with respect thereto.

Hieda fails to disclose or suggest the adhesion film required by claim 1. In the Fig. 30B embodiment of Hieda for example, there is clearly no adhesion film provided between the oxide layer 59 and the electrode material for Ru 60 provided thereover (see Figs. 30B-30C; and col. 21, lines 21-42). Because Hieda fails to disclose or suggest the

adhesion film required by claim 1, Hieda also cannot achieve the advantages discussed above with respect thereto of improved adhesion between the electrode material and the insulation layer. Hieda is unrelated to this aspect of claim 1.

Moreover, the TiO_2 barrier layer mentioned in Nishioka at col. 5, lines 43-45 is entirely unrelated to the invention of claim 1. The TiO_2 barrier layer of Nishioka is deposited over an oxide layer, for the sole purpose of providing a "barrier" against diffusion during heat treatment or the like. In other words, the TiO_2 layer of Nishioka must necessarily remain in place in the final product in order to perform its "barrier" against diffusion function. In contrast, the adhesion layer called for in claim 1 is *removed* during the process of manufacture as expressly stated in amended claim 1. Nishioka thus teaches the exact opposite of what claim 1 requires, and cannot possibly be cited against the invention of claim 1 in this respect.

Claim 4

Claim 4 also stands rejected under 35 U.S.C. Section 102(e) as being allegedly anticipated by Hieda. This Section 102(e) rejection of claim 4 is respectfully traversed for at least the following reasons.

First, it is pointed out that Hieda fails to disclose or suggest the "adhesion layer" recited in claim 4 for the reasons discussed above.

Second, Hieda fails to disclose or suggest forming "a second insulation film on the first conductive film so as to fill the hole" as required by claim 4. For example, see second insulation film 28 in the Fig. 2 embodiment of the instant application. In contrast with the invention of claim 4, in Fig 24 of Hieda layer 26 cannot possibly be considered

the claimed second insulation film because it does not fill the hole defined by the cup-shaped electrode 24. Moreover, if one were to incorrectly contend that layer 26 did fill the hole defined by the cup-shaped electrode 24 (this contention would be incorrect), then the "dielectric film" limitation recited later in claim 4 would not be met. Furthermore, the Figure 24 embodiment of Hieda also fails to disclose or suggest etching the second insulation film (which fills the hole) until an upper surface of the first conductive film is reached. In contrast, Hieda's layer 26 remains in place and is not removed over a surface of an underlying conductive film as required by claim 4. It can be seen that the Figure 24 embodiment of Hieda is entirely unrelated to the invention of claim 4. The §102(e) rejection of claim 4 lacks merit and should be withdrawn.

Finally, applicant would like to point out that it is well established that a §102(e) rejection of a particular claim cannot be established by combining multiple embodiments from a given reference.

For at least the foregoing reasons, it is respectfully requested that all rejections be withdrawn. All claims are in condition for allowance. If any minor matter remains to be resolved, the Examiner is invited to telephone the undersigned with regard to the same.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: _____
Joseph A. Rhoa
Reg. No. 37,515

JAR:caj
1100 North Glebe Road, 8th Floor
Arlington, VA 22201-4714
Telephone: (703) 816-4000
Facsimile: (703) 816-4100

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

1. (Amended) A method of producing a semiconductor device, the method comprising:

sequentially forming an interlayer insulating film and a barrier film on a semiconductor substrate;

making a contact hole in the barrier film and the interlayer insulating film[at the same time], and forming a plug within the contact hole;

forming an insulation film and then an adhesion film on the plug and the barrier film, and then forming a hole in the insulation film and the adhesion film leading to the plug such that an upper surface of the plug and an adjacent part of the barrier film are exposed;

forming a first conductive film on the insulation and adhesion films and on and over an exposed part of the barrier film in the hole such that the hole in the insulation film and in the adhesion film is filled with the first conductive film, and then etching the first conductive film and the adhesion film by a chemical mechanical polishing method to thereby form a lower electrode within the hole in the insulation film;

etching the insulation film until the barrier film is exposed, so as to leave the lower electrode in a protuberant manner;

wherein the adhesion film is removed before the lower electrode is left in the protuberant manner;

forming a dielectric film that covers the protuberant lower electrode and at least part of the barrier film, and then forming a second conductive film that covers at least part of the dielectric film, said dielectric film being made of a ferroelectric or high-dielectric-constant substance; and

patterning the dielectric film and the second conductive film simultaneously to thereby form a capacitor dielectric film and an upper electrode.

3. (Amended) The method according to claim 1, [further comprising, after forming the insulation film, forming]wherein said adhesion film comprises a Ti film or a TiO_2 film on the insulation film.

4. (Amended) A method of producing a semiconductor device, the method comprising:

sequentially forming an interlayer insulating film and a barrier film so as to be supported by a semiconductor substrate;

making a contact hole in the barrier film and the interlayer insulating film [at the same time]and forming a plug within the contact hole;

forming a first insulation film and then an adhesion film on the plug and the barrier film, and then forming a hole leading to the plug in the first insulation film and the adhesion film such that an upper surface of the plug is exposed;

forming a first conductive film over at least part of the first insulation film and adhesion film and within the hole such that the first conductive film within the hole does

not fill the hole but covers surfaces defining the hole, and then forming a second insulation film on the first conductive film so as to fill the hole;

etching the second insulation film until an upper surface of the first conductive film is reached, and then etching the first conductive film, the adhesion film, and the second insulation film in the hole by a chemical mechanical polishing method until the first insulation film is exposed, to thereby form a cup-shaped lower electrode within the hole;

etching the first insulation film and the second insulation film within the hole until the barrier film and the lower electrode are exposed, respectively;

forming a dielectric film over the cup-shaped lower electrode such that the dielectric film covers inner and outer peripheries and an inner bottom surface of the cup-shaped lower electrode, and then forming a second conductive film that covers the dielectric film, said dielectric film being made of a ferroelectric or high-dielectric-constant substance; and

patterning the dielectric film and the second conductive film simultaneously to thereby form a capacitor dielectric film and an upper electrode.

6. (Amended) The method according to claim 4, [further comprising, after forming the first insulation film, forming]wherein the adhesion film comprises a Ti film or a TiO_2 film on the first insulation film.